Ultra-Thin-Body Self-Aligned InGaAs MOSFETs on Insulator (III-V-O-I) by a Tight-Pitch Process

Jianqiang Lin, Lukas Czornomaz*, Nicolas Daix*, Dimitri A. Antoniadis, and Jesús A. del Alamo
Microsystems Technology Laboratories, Massachusetts Institute of Technology, 60 Vassar St., Rm. 39-619, Cambridge, MA, 02139 USA.
*IBM Zurich Research Laboratory, Säumerstrasse 4, 8803 Rüschlikon, SWITZERLAND.
E-mail: LINJQ@mit.edu. Phone: 1-617-253-0714. Fax: 1-617-324-5341.

Abstract

We report a self-aligned InGaAs Quantum-Well MOSFET (QW-MOSFET) on III-V-O-I substrate fabricated through a tight-pitch process. The ultra-thin body (UTB) III-V-O-I layer structure was fabricated on Si through a direct bonding technique. The III-V MOSFETs, with a self-aligned gate and metal contacts, were fabricated by a gate-last method. For the first time, we demonstrate adjacent devices with contact metal spacing of 150 nm. The fabrication features CMOS compatibility with a wet-etch free, lift-off free and Au-free process in the front end. Transport and short-channel effects (SCE) are studied as a function of back bias. Excellent SCE control is obtained with DIBL and subthreshold swing benchmarked against state-of-the-art III-V-O-I data. The reported technology provides a new path to integrate III-V front-end devices for future high density circuit applications.

Introduction

InGaAs is a promising channel material candidate for future CMOS applications **[1]**. Great progress has recently taken place in III-V MOSFET research, including advances in performance and 3D device architectures suitable for scaling **[2-4]**. Efforts have also been devoted to exploring III-V MOSFET integration schemes onto a Si substrate. In this regard, UTB III-V-O-I substrate approaches have received recent attention **[5-12]**. To date, there are still very few studies on III-V-O-I device prototypes fabricated through Si CMOS compatible processes. Besides, the architecture has not achieved full self-alignment and cannot deliver high device density. In this work, we demonstrate a Si-compatible self-aligned process to fabricate high density InGaAs QW-MOSFETs on insulator.

Fabrication

III-V-O-I substrate fabrication (**Fig. 1a**): The III-V heterostructure is grown by MBE on semi-insulating InP and comprises of, in order of growth, a highly doped n^+ capping layer, an InP etch stopper, a strained $In_{0.7}Ga_{0.3}As$ channel and a thin InAlAs buffer layer that is Si δ-doped to N_s=1x10^{12} cm^{-2} at its middle. A 30 nm-thick Al_2O_3 BOX layer is deposited by ALD on the III-V donor wafer. The thin InAlAs buffer acts as a barrier which prevents carriers from the channel to be affected by the traps present at the III-V/BOX interface as in **[5]**. After wet cleaning, the III-V donor wafer is bonded to a p^+-Si substrate whose doping (N_A=1x10^{18} cm^{-3}) is selected to act as a ground plane. Substrate fabrication is completed by wet removal of the donor InP wafer. **Figs. 2(a,b)** summarize structural data, including XRD and AFM, acquired at the end of UTB III-V-O-I substrate fabrication. AFM data confirm the excellent surface quality. The thin III-V device heterostructure on insulator on Si is described in **Fig. 3**.

Device fabrication (**Fig. 1b**): The schematic of the final device is shown in **Fig. 3**. This is a contact-first, gate-last process with intrinsic and access regions created by a 3-step gate recess process that results in a highly-conducting ledge **[2]**. The gate, channel, ledge and contacts are fully self-aligned. Using a 30 nm ledge length, this process allows us to closely pack the device with 150 nm gate/contact pitch, as shown in the cross section in **Fig. 4(a)**. This is the smallest gate/contact pitch dimension of any III-V-O-I prototype device to date **[5]**. The cross section of a device with L_g=50 nm and L_{ledge}=30 nm is shown in **Fig. 4(b)**. The non-alloyed Mo contact used here has much lower R_{sh} (5 Ω/□ for t=30 nm) than the more commonly used Ni-InGaAs alloyed contacts (R_{sh}~42 Ω/□ for 30 nm) **[8]**. High metal R_{sh} constitutes the major component of the Ni-InGaAs contact scheme in **[8]**. The n^+ caps form raised S/D contacts. Our 3-step recess process allows us to trim the intrinsic channel thickness down to 8 nm. We use 3.5 nm ALD HfO_2 as gate dielectric directly on InGaAs (EOT=0.7 nm). Isolated devices with long contacts are used for electrical measurements.

Results and discussion

The subthreshold characteristics of long devices with or without forming gas anneal (FGA) are shown in **Fig. 5**. V_t shifts positively due to FGA ($V_{t,sat}$=35 mV defined at V_{ds}=0.5 V and 1μA/μm), making them enhancement-mode devices. FGA also improves the subthreshold swing (S) and DIBL (DIBL extracted from steep swing region). However, the device drive current is relatively low due to a high series resistance (R_{sd}).

The original of this can be understood from **Fig. 6** which shows long-channel V_t at V_{ds}=0.5 V and total source and drain resistance R_{sd} (extracted by gate length extrapolation method) as a function of back bias V_{bs}. A relatively large swing in V_t (ΔV_t =200 mV) is achieved for V_{bs}=±4 V. Significant R_{sd} modulation is also observed. With V_{bs}=0 and an E-mode device, the access regions have relatively low N_s. With positive V_{bs}, V_t shifts negatively, N_s in the extrinsic region increases and R_{sd} improves. The lowest R_{sd} is ~520 Ω.μm at V_{bs}=4 V. This R_{sd} is still significantly higher than our previous work on an InP wafer with a similar extrinsic region except for thicker caps **[2]**. R_{sd} improvement can be achieved by thickening the cap and optimizing the ledge design for this III-V-O-I structure.

The study of the transistor's electrical characteristics as a function of V_{bs} reveals interesting device design issues. **Figs. 7** and **8** show the output and transconductance characteristics for a L_g=70 nm device as a function of V_{bs}. With positive V_{bs}, R_{sd} improves and the transconductance increases. The device also delivers higher ON current. **Fig. 9** shows the subthreshold characteristics of a device with L_g=70 nm at three V_{bs}. With positive V_{bs}, S becomes softer but DIBL markedly improves. S and DIBL as a function of V_{bs} are shown in **Fig. 10**. The larger S for positive V_{bs} is due to the deeper location of the electron channel. On the contrary, DIBL improves with positive V_{bs}. This could be due to a reduction in the extent of a depletion region at the surface of the p-type Si wafer bringing the ground plane closer to the channel.

Split C-Vs are shown in **Fig. 11** by a two-FET subtraction method. Very low frequency dispersion is observed. CET (at V_{g-sd}=1 V) is 2 nm. The gate leakage current density is very low, as shown in the inset, suggesting that further dielectric scaling is possible. The impact of back gate modulation on channel mobility is shown in **Fig. 12**. The mobility is corrected for series resistance. A significantly lower mobility is observed at negative V_{bs}. This could be due to Coulomb scattering from the back interface and delta-doped layer as the electron concentration at the bottom of the channel is reduced and the confinement increases.

Figs. 13 and **14** show S and DIBL as a function of L_g, benchmarked with the recently published MOSFETs on III-V-O-I. S and DIBL are extracted at V_{bs}=0 V. In addition, S is extracted at V_{ds}=0.5 V. Our long-channel device shows the lowest S of 83 mV/dec in the L_g~1 μm regime. S matches the lowest reported values in the sub-100 nm L_g regime. DIBL also matches the lowest values in the sub-100 nm L_g regime. Our UTB III-V-O-I devices demonstrate the combination of both low S and DIBL from L_g=1 μm down to 50 nm, indicating excellent electrostatic control. **Fig. 15** shows the mobility at N_s=7x10^{12} cm^{-2} against channel thickness (t_{ch}) for different values of V_{bs}. At t_{ch}=8 nm, our device shows the highest mobility for V_{bs}=0 when compared with other works. The design of the InAlAs buffer underneath the channel helps to minimize scattering from the back III-V/BOX interface.

Conclusions

We report a self-aligned InGaAs Quantum-Well MOSFET (QW-MOSFET) on III-V-O-I substrate that features a tight contact pitch. Prototype structures with a contact pitch of 150 nm are demonstrated. Benchmarking shows the devices from this work have combination of both low S and DIBL from L_g=1 μm to 50 nm, indicating excellent electrostatic control. A study of the impact of applying a back bias reveals the considerable potential for optimization of this structure.

(a) III-V-O-I substrate

- III-V epi on InP by MBE
- Al_2O_3 BOX depo on III-V
- p-Si and III-V wet clean
- Direct wafer bonding
- InP donor wafer removal

(b) Device fabrication

- W/Mo contact & SiO_2 depo
- Gate E-beam lithography
- 3-step gate recess [2]
- HfO_2 gate deposition
- Mo gate depo and etch
- Pad formation
- FGA 300°C 15 min

Fig. 1. Process flow for: (a) Substrate preparation, (b) Self-aligned InGaAs MOSFET fabrication.

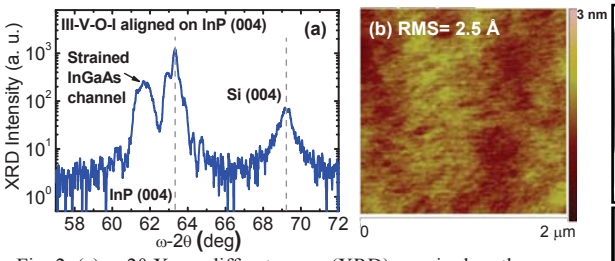
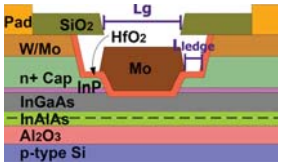


Fig. 2. (a) ω-2θ X-ray diffractogram (XRD) acquired on the finished III-V-O-I substrate and aligned on the InP (004) peak. (b) AFM scan of the surface of the III-V-O-I substrate.



Structure	Composition	t
Metal contact	W/Mo	30 nm*
Gate dielectric	HfO_2	3.5 nm
Intrinsic channel	$In_{0.7}Ga_{0.3}As$	8 nm
Buffers	InAlAs	10 nm
BOX	Al_2O_3	30 nm

*R_{sh} = 5 Ω/□

Fig. 3. Complete device structure with dimensions.

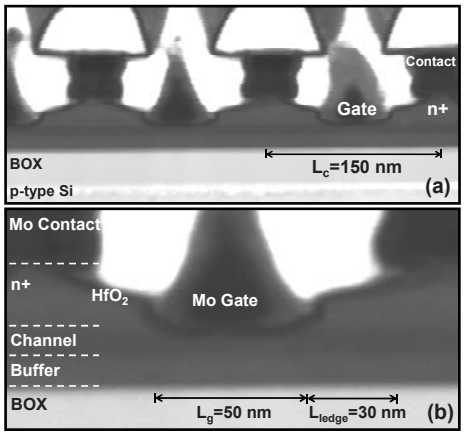


Fig. 4. STEM cross sectional for: (a) MOSFETs with gate/contact pitch of L_c = 150 nm on III-V-O-I, (b) L_g= 50 nm device with L_{ledge}=30 nm.

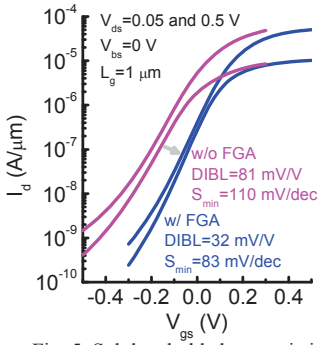


Fig. 5. Subthreshold characteristics of MOSFET with L_g=1 μm at V_{bs}= 0 V before and after FGA.

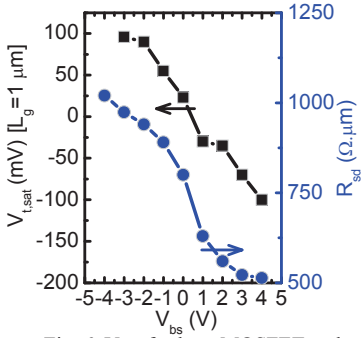


Fig. 6. $V_{t,sat}$ for long MOSFET and R_{sd} *vs.* V_{bs} (V_t defined at V_{ds}=0.5 V and I_d=1 μA/μm).

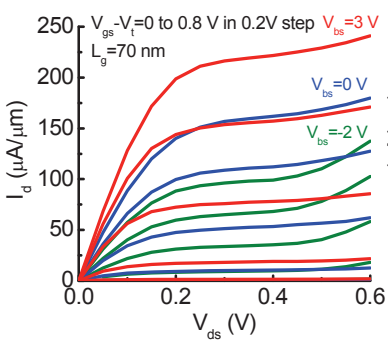


Fig. 7. Output characteristics of MOSFET with L_g=70 nm at different V_{bs}.

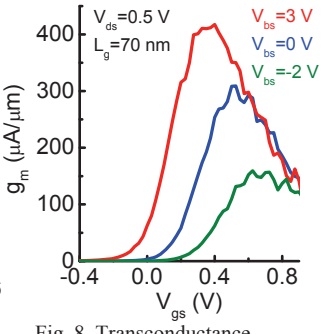


Fig. 8. Transconductance characteristics of MOSFET with L_g=70 nm at different V_{bs}.

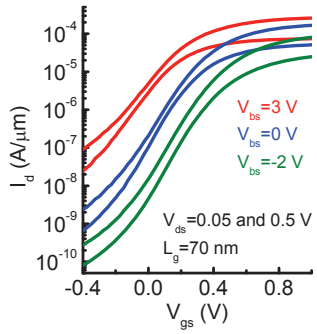


Fig. 9. Subthreshold characteristics of MOSFET with L_g=70 nm at different V_{bs}.

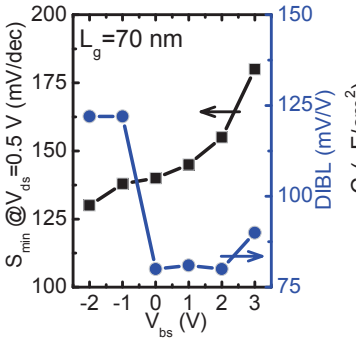


Fig 10. Subthreshold swing and DIBL for MOSFET with L_g= 70 nm *vs.* V_{bs}.

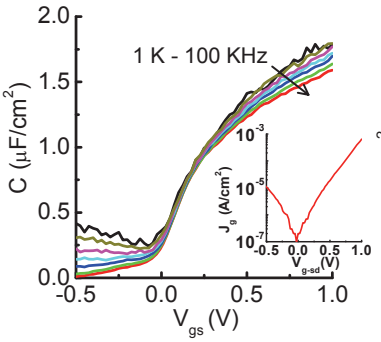


Fig. 11. Split-CVs at V_{bs}= 0 V by two-FET subtraction method. Inset shows gate leakage current density.

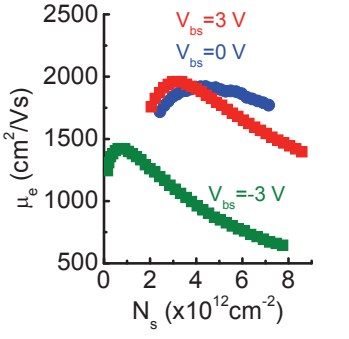


Fig. 12. Mobility extracted from long-channel MOSFET at different V_{bs}. R_{sd} correction is applied.

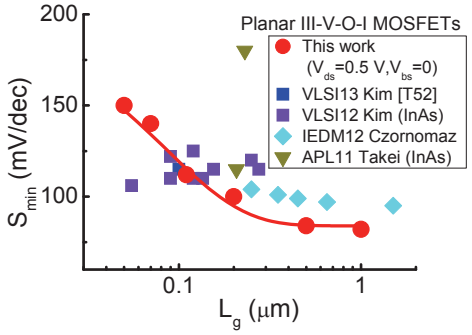


Fig. 13. S_{min} *vs.* L_g for this work and recently published III-V MOSFETs on insulator.

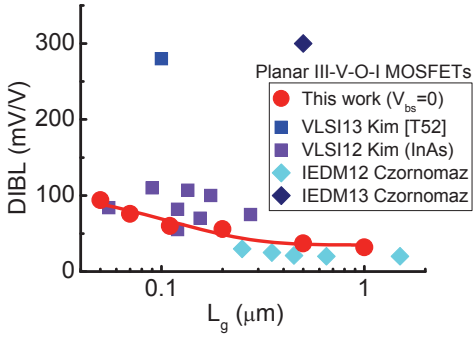


Fig. 14. DIBL *vs.* L_g for this work and recently published III-V MOSFETs on insulator.

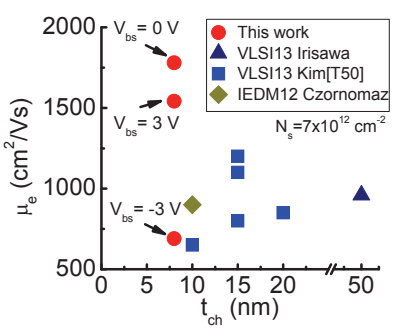


Fig. 15. μ_e *vs.* t_{ch} for this work and recently published III-V MOSFETs on insulator.

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Reference: [1] J. A. del Alamo, *et al.,* IEDM 2013, p.24. [2] J. Lin, *et al.* , IEDM 2013, p.421. [3] S. Lee, *et al.,* Applied, Physics Lett., Vol. 103, p. 233503 (2013). [4] T.-W. Kim, *et al.,* IEDM 2013, p. 425. [5] L. Czornomaz, *et al,* IEDM 2012, p. 517. [6] L. Czornomaz, *et al,* IEDM 2013, p. 517. [7] S. H. Kim, *et al,* VLSI 2013, p.T50. [8] S. H. Kim, *et al,* VLSI 2013, p.T52. [9] S. H. Kim, *et al,* VLSI 2012, p.177. [10] K. Takei, *et al.,* Applied, Physics Lett., Vol. 102, p. 153513 (2013). [11] K. Takei, *et al.,* Applied, Physics Lett., Vol. 99, p. 103507 (2011). [12] T. Irisawa, *et al,* VLSI 2013, p. T55.